tric **18** that is located directly beneath the sacrificial gate **20** is removed from the structure. The removal of the sacrificial gate **20** and the gate dielectric **18** beneath the sacrificial gate **20** provides an opening **26** which exposes a surface of the semiconductor substrate **12**. The resultant structure that is formed after this step of the present invention has been performed is shown, for example, in FIG. **3**B. Depending on the materials of the sacrificial gate **20** and the gate dielectric **18**, various suitable processes can be used to remove those materials. For example, a wet etching process with an etchant containing ammonia-based chemistry or a dry etching process such as a plasma etch with an etchant containing sulfuric fluoride can be used to remove the sacrificial gate **20** comprising polysilicon. A wet etching process with an etchant of hydrofluoride acid can be used to remove the gate dielectric **18** comprising silicon oxide.

[0067] Next, a U-shaped high-k gate dielectric **28** is formed within the opening **26** and thereafter a metal-containing conductor **30** is formed on the exposed surfaces of the U-shaped high-k gate dielectric **28** providing the structure shown, for example, in FIG. **3**C. The U-shaped high-k gate dielectric **28** comprises any dielectric material whose dielectric constant is greater than 4.0, typically greater than 7.0. Examples of such high-k gate dielectric materials include but are not limited to TiO_2, Al_2O_3, ZrO_2, HfO_2, Ta_2O_5, La_2O_3, mixed metal oxides such a perovskite-type oxides, and combinations and multilayers thereof. Silicates and nitrides of the aforementioned metal oxides can also be used as the high-k gate dielectric material. Optionally, a first interfacial layer (not shown) can be formed at the interface between the U-shaped high-k gate dielectric **28** and the substrate **12** to improve device characteristics such as reducing interface traps. The first interfacial layer, if present, may comprise silicon oxide, silicon nitride, or oxynitride and can be formed by thermal oxidation, chemical oxidation, thermal nitridation, and chemical nitridation. Furthermore, a second interfacial layer (not shown) can be deposited at the top or within the U-shape high-k dielectric **28** before forming the metal-containing gate conductor **30**. The second interfacial layer, if present, helps optimize device characteristics by adjusting the work function, and/or stabilizing the flatband voltage and threshold voltage. The second interfacial layer, if present, may comprise a rare earth-containing layer comprising La_2O_3, LaN, or any other suitable materials. The U-shaped high-k gate dielectric **28** can be formed by a conventional deposition process, including but not limited to, atomic layer deposition (ALD), chemical vapor deposition (CVD), low-pressure chemical vapor deposition (LPCVD), plasma enhanced chemical vapor deposition (PECVD), rapid thermal chemical vapor deposition (RTCVD), limited reaction processing CVD (LRPCVD), ultrahigh vacuum chemical vapor deposition (UHVCVD), metalorganic chemical vapor deposition (MOCVD), molecular beam epitaxy (MBE), physical vapor deposition, ion beam deposition, electron beam deposition, and laser assisted deposition.

[0068] The U-shaped high-k gate dielectric **28** has a thickness that is less than that of the remaining outer portions of the gate dielectric **18**. Typically, the U-shaped high-k gate dielectric **28** has a thickness from about 1 to about 20 nm, with a thickness from about 2 to about 10 nm being even more typical.

[0069] The metal-containing gate conductor **30** is formed utilizing a conventional deposition process such as, for example, atomic layer deposition (ALD), chemical vapor deposition (CVD), metalorganic chemical vapor deposition (MOCVD), molecular beam epitaxy (MBE), physical vapor deposition, sputtering, plating, evaporation, ion beam deposition, electron beam deposition, laser assisted deposition, and chemical solution deposition. The metal-containing gate conductor **30** includes a conductive metal such as, but not limited to Al, W, Cu, Pt, Ag, Au, Ru, Ir, Rh and Re, alloys of a conductive metal, e.g., Al—Cu, silicides of a conductive metal, e.g., W silicide, and Pt silicide, nitrides of a conductive metal, e.g., AlN, and combinations and multilayers thereof. A conventional planarization process such as chemical mechanical polishing (CMP) can be used to remove any metal-containing gate conductor **30** that is deposited at the top of the interlevel dielectric **24** and the sacrificial spacer **22**. A conventional etch process such as a wet etch or dry etch can be used to remove any U-shaped high-k gate dielectric **28** that is deposited at the top of the interlevel dielectric **24** and the sacrificial spacer **22**.

[0070] Next, and as shown in FIG. **3**D, the sacrificial spacer **22** is removed from the structure exposing the remaining outer portions of the gate dielectric **18**, outer sidewalls of the U-shaped high-k gate dielectric **28**, and sidewalls of the interlevel dielectric material **24**. The sacrificial spacer **22** is removed utilizing an etching process that selectively removes the material of the sacrificial spacer **22** as compared with the interlevel dielectric material **24** and the remaining gate dielectric **18**. An example of such an etching process that can be used includes a wet etch process with an etch etchant containing phosphoric acid or a mix of hydrofluoric and ethylene glycol (HF/EG) to remove the sacrificial spacer **22** which is formed of silicon nitride. Alternatively, the sacrificial spacer **22**, when it comprises silicon nitride, can be removed by a dry etch process such as a chemical downstream etch (CDE).

[0071] FIG. **3**E shows the structure that is formed after removing the U-shaped high-k gate dielectric **28** from substantially all of the vertical sidewalls of the metal-containing gate conductor **30**. The presence of the thicker gate dielectric **18** ensures that a substantially complete removal of the high-k gate material from the metal-containing gate sidewalls is obtained without undercutting the high-k gate dielectric material that is located beneath the metal-containing gate conductor **30**. Removing substantially all of the high-k gate dielectric material from the vertical sidewalls of the metal-containing gate conductor **30** reduces the contact-to-gate conductor capacitance.

[0072] It is noted that some portion of the U-shaped high-k gate dielectric **28** however remains on the vertical sidewalls of the metal-containing gate conductor **30** covering the gate corners at the base segment of the metal-containing gate conductor **30**. The gate corners are labeled by reference numeral **31** in FIG. **3**E. In the present invention, the high-k gate material that remains at the gate corners **31** has a height that is less than the height of the remaining gate dielectric **18**.

[0073] The removal of the U-shaped high-k gate dielectric **28** from substantially all of the vertical sidewalls of the metal-containing gate conductor **30** is performed utilizing an etching process that selectively removes the high gate dielectric material relative to that of the other materials that are exposed to the etching process. An example of such an etching process includes a boron-halogen plasma which comprises a boron-halogen compound (e.g., BCl_3) and nitrogen. Alternatively, the high-k gate dielectric **28** can be removed from the vertical